

Remarks

Favorable reconsideration of this application is requested in view of the following remarks. For the reasons set forth below, Applicant respectfully submits that the claimed invention is allowable over the cited references.

The non-final Office Action dated March 9, 2005, indicated that claims 7-24 are allowed; claims 2 and 29 would be allowable if rewritten; the drawings are objected to; claims 2, 27, 29 and 32 are objected to due to informalities; claims 1-4, 6, 27-29 and 32 are rejected under 35 U.S.C. § 112(2); claims 1, 26-28, 31 and 32 are rejected under 35 U.S.C. § 102(e) over Bremer (U.S. Patent No. 6,160,790); claims 27 and 32 are rejected under 35 U.S.C. § 103(a) over Sakurai *et al.* (U.S. Patent No. 5,594,756); and claims 3, 4 and 6 are rejected under 35 U.S.C. § 103(a) over Bremer in view of applicant's background of the invention.

Applicant appreciates the allowance of claims 7-24.

Applicant respectfully traverses the drawing objection because the drawings show every feature specified in the claims. First, the Examiner identifies a "step/means for iteratively computing a probable cross talk signal." Applicant submits that these limitations are already shown, for example, in Fig. 3 (*e.g.*, step 305). The iterative process is illustrated, for example, by blocks 303-307 of Fig. 3. Next, the Examiner identifies a "step or means for calculating the data based on the iteratively computed probable cross talk converging toward the superimposed cross talk." One illustration of this may also be found, for example, at block 305 of Fig. 3. Finally, the Examiner identifies a "means/step for computing a probable desired signal estimate." An example of this may also be found in block 305 of Fig. 3 as well as in Fig. 4, which is a flow diagram of the relevant steps involved in calculating expected values for each symbol in the symbol block for block 305. Applicant also notes the discussion at page 14, lines 19-32, indicating the various functions performed at step 305 of Fig. 3. As each of the identified limitations has been shown to be present in the figures, Applicant submits that the objection to the drawings is improper and requests that the objection be removed.

Regarding the objections to claims 27, 29 and 32, Applicant respectfully traverses because the Examiner's suggestions are not consistent with the claimed invention. Each of the objections address limitations directed to results of an iterative process. As discussed at

page 13 of the Specification, one example process includes an initial estimate of a cross-talk signal that is refined through iterative calculations to obtain a cross-talk signal that more closely resembles the actual value. *See* page 13, lines 7-28. Applicant submits that the term “converging” must apply to a plurality of things, *e.g.*, signals, as one item cannot converge, as claimed. Thus, the singular use of the term “signal” or “estimate” in the respective objected-to claims refers to one iterative result while the plural use of the term refers to the iterative results as a whole. Applicant submits that the claim language is appropriate as viewed by a skilled artisan and requests that the objections be withdrawn.

Applicant respectfully traverses the Section 112(2) rejections because the claim language particularly points out the subject matter of the instant invention. The Examiner asserts that it is unclear “how a plurality of probable cross talk signals will converge toward a single signal (superimposed cross talk) as the plurality of probable cross talk signals are generated as a result of refining a previous probable cross talk into a better probable cross talk.” Applicant submits that the skilled artisan would recognize that “convergence” occurs when multiple items meet or approach a specified designation. One example definition of “convergence” is provided in a paper published on the North Carolina State University web site at: <http://www2.chass.ncsu.edu/garson/pa765/multilevel.htm>. The question “What is ‘convergence’?” is answered with respect to multiple items (*i.e.*, “stable estimates”):

Maximum likelihood estimation (MLE) is an iterative algorithm which may take many passes on the data to reach stable coefficient estimates. In some cases no convergence on stable estimates is reached even after a large number of iterations. Lack of convergence generally indicates the model is badly misspecified and must be thrown out, but it may also be due to too small a sample. Misspecification is often associated with trying to estimate random (base-level) coefficients which are close to or equal to zero, which in turn leads to lack of convergence.

Another example of convergence in a linear system may be found in the attached page 387 of Appendix A found at: <http://www.intusoft.com/lit/IsSpice4.pdf>.

Further, the Dictionary of Electronics defines “convergence” as, “In a multibeam electron tube, such as a colour picture tube, the intersection of the beams at a specified point.” *See, Dictionary of Electronics Second edition*, edited by Valerie Illingworth, Penguin Books, 1988, page 94, attached as Exhibit B. Each of these

examples identify multiple items (*e.g.*, coefficients, mesh currents, and beams) approaching a desired outcome or location. Thus, the claimed iteratively computed probable cross talk signals converge toward the (actual or true) superimposed cross talk signal. Applicant therefore submits that the skilled artisan would recognize that the claim language clearly sets forth the instant invention. Applicant accordingly requests that the Section 112(2) rejection be withdrawn.

With particular respect to claims 27 and 32, Applicant traverses the Section 112(2) rejection. Applicant submits that the claim language should implicitly be understood to identify that the iteratively computed probably cross talk signals are converging toward the superimposed cross talk signal. However, in an effort to facilitate prosecution, Applicant has amended claims 27 and 32 in accordance with the Examiner's suggestion. Thus, Applicant submits that the Section 112(2) rejection is moot and the rejection should be withdrawn.

With respect to the objection to claims 2 and 29, Applicant has amended both of the claims. Applicant has amended claims 2 and 29 to change "estimate" to "signal" to be consistent with the underlying claims and, in claim 2, changed "estimate" to "estimates" in line 2 to provide proper verb agreement. In view of the above discussion, Applicant submits that the objection is overcome and requests that the objection be removed.

Applicant respectfully traverses each of the prior art rejections (Section 102(e) and 103(a)) that rely on the '790 reference because the Examiner fails to present a reference that corresponds to the claimed invention. The '790 reference fails to teach iteratively computing a probable cross-talk signal, as claimed. The '790 reference fails to make any mention or use of the word "iterate" or any variation thereof. The Examiner's assertion that in order for the receiver to be free of cross-talk, the cancellation signal has to resemble/converge toward the superimposed cross-talk signal is erroneous. The Examiner appears to incorrectly use the terms "resemble" and "converge" interchangeably; however, the terms do not mean the same thing. For example, the noise in a receiver could be steady-state and simply be subtracted to provide a receiver free of cross-talk. As another example, the noise could be subtracted in a feedback loop as discussed below in connection with the '756 reference. Further, the Examiner's citation to elements 21a-d in Fig. 5 as representing

iterations is unfounded as elements 21a-d represent separate cross-talk cancellers associated with each of N separate transmitters 12a-d. *See, e.g.*, column 6, lines 32-37. Thus, the '790 reference fails to teach any iteration, as claimed. Without a presentation of correspondence to each of the claimed limitations, the prior art rejections are improper and cannot be maintained. Applicant accordingly requests that the rejections be withdrawn.

Applicant also traverses the Section 103(a) rejection of claims 27 and 32 because the Examiner fails to present a reference that corresponds to the claimed invention. The '756 reference also fails to teach iteratively computing a probable cross-talk signal, as claimed. The Examiner's assertion that "the noise portion is iteratively computed because of the presence of the feedback path" is untrue. The '756 reference teaches that the feedback signal and the FFF signal at a particular sample time are summed by subtracter 4 (of Fig. 4). At a subsequent sample time, subtracter 4 again sums the FFF signal and the feedback signal; however, the subsequent summation is independent of the previous sample's summation. Therefore, the '756 system fails to teach an iteration as claimed. Moreover, the '756 reference fails to make any mention or use of the word "iterate" or any variation thereof. Without a presentation of correspondence to each of the claimed limitations, the Section 103(a) rejection cannot be maintained and Applicant requests that the rejection be withdrawn.

The Examiner erroneously asserts at pages 6-7, that in order for the superimposed interference to be removed or canceled from the received signal, the estimate interference would inherently have to be as close as possible to the superimposed interference and it is also an indication of convergence. Applicant respectfully traverses because the Examiner's assertion is unsupported and incorrect. In order to establish inherency, the extrinsic evidence "must make clear that the missing descriptive matter *is necessarily present in the thing described in the reference*, and that it would be so recognized by persons of ordinary skill." *Continental Can Co. v. Monsanto Co.*, 948 F.2d 1264, 1268, 20 U.S.P.Q.2d 1746, 1749 (Fed. Cir. 1991) (emphasis added). "Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient." *Id.* at 1269, 20 U.S.P.Q.2d at

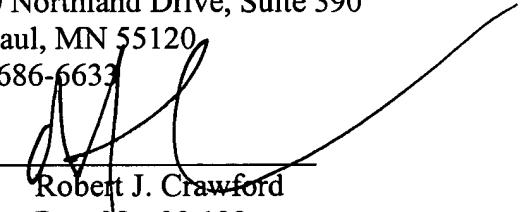
1749 (quoting *In re Oelrich*, 666 F.2d 578, 581, 212 U.S.P.Q. 323, 326 (C.C.P.A. 1981). *See also*, MPEP § 2112. The Office Action fails to provide any of the requisite evidence in support of the inherency assertion. The Examiner has failed to identify any teachings in the '756 reference directed to calculating the data signal based at least in part upon the iteratively computed probable cross talk signal resembling the superimposed cross-talk signal. In contrast to the Examiner's inherency conclusion and as discussed above, the '756 system appears to be directed to a system that merely subtracts interference from the received signal without any use of an iterative process. *See, e.g.*, Fig. 4. Accordingly, the inherency argument is unsupported and incorrect and therefore cannot be maintained.

In view of the above discussion, Applicant believes that each of the rejections has been overcome and the application is in condition for allowance. A favorable response is requested. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is encouraged to contact the undersigned at (651) 686-6633.

Respectfully submitted,

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By: 
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Reg. No. 32,122

Appendices

Appendix A: Solving SPICE Convergence Problems

*See the
Convergence
Wizard for more
help with
solving
convergence
problems.*

The following techniques on solving convergence problems are taken from various sources including:

- [1] Meares, L.G., Hymowitz C.E. "SIMULATING WITH SPICE", Intusoft, 1988
- [2] Muller, K.H. "A SPICE COOKBOOK", Intusoft, 1990
- [3] Meares, L.G., Hymowitz C.E. "SPICE APPLICATIONS HANDBOOK", Intusoft, 1990
- [4] *Intusoft Newsletters*, various dates from 1986 to present
- [5] The Designer's Guide to SPIC and Spectre, Kenneth S. Kundert, Kluwer Academic Publishers, 1995
- [6] The SPICE Book, Andrei Vladimirescu, John Wiley & Sons Inc., 1994
- [7] Inside SPICE, Ron Kielkowski, McGraw-Hill, Inc. 1994

What is Convergence? (or in my case, Non-Convergence)

The answer to a nonlinear problem, such as those in the SPICE DC and Transient analyses, is found via an iterative solution. For example, IsSpice4 makes an initial guess at the circuit's node voltages and then, using the circuit conductances, calculates the mesh currents. The currents are then used to recalculate the node voltages, and the cycle begins again. This continues until all of the node voltages settle to values that are within specific tolerance limits. These limits can be altered using various .Options parameters such as Reltol, Vntol, and Abstol.

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the case of a planar configuration where the final direction of current flow is parallel to the plane of the metal (see diagram), the contact resistance is defined to be the resistance between the metal and an imaginary plane at the edge of and perpendicular to the metal, and the *transfer length*, L_t , is the distance from the edge of the metal at which the current in the semiconductor has fallen to 1/e of its original value.

If the conductors are made from two different materials a difference of potential will arise when they are placed in contact. This *contact potential* results from a difference in the work functions of the two materials and is usually of the order of a few tenths of a volt. If the contact is made between two semiconductors of different polarities or between a metal and a semiconductor, a built-in field will be produced with an associated contact resistance to current flow. See also p-n junction; Schottky barrier.

contact lithography See photolithography.

contactor A type of switch used for the automatic making and breaking of a circuit and designed for frequent use.

contact potential See contact.

contact resistance See contact.

continuous duty See duty.

continuous loading See transmission line.

continuous-wave radar See radar.

continuous X-rays See X-rays.

contrast control See television receiver.

control characteristic See thyatron.

control circuit See transistor.

control electrode An electrode to which a signal is applied in order to produce changes in the currents of one or more of the other electrodes. In a bipolar transistor with common-emitter connection the base electrode is the control electrode; the gate electrode is the control electrode of a field-effect transistor; in a thermionic valve it is the *control grid*; in a cathode-ray tube it is the *modulator electrode*.

control grid See control electrode; thermionic valve.

controlled-carrier modulation See floating-carrier modulation.

control ratio Syn. grid control ratio. See thyatron.

control unit See central processing unit.

convergence In a multibeam electron tube, such as a colour picture tube, the intersection of the beams at a specified point. Convergence may be achieved electrostatically using a *convergence electrode* or electromagnetically using a *convergence magnet*. When scanning of the beams across the screen of the tube is carried out, the surface generated by the point of intersection of two or more of the electron beams is the *convergence surface*.

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convergence coils See colour picture tube.

conversion conductance See mixer.

conversion gain ratio See frequency changer.

conversion transducer See frequency changer.

conversion voltage gain See frequency changer.

converter (1) A device for converting alternating current to direct current or vice versa.

(2) A device that changes the frequency of a signal; a *frequency changer*.

(3) A device, such as an impedance converter, that has different electrical properties at its input and output and may be used to couple dissimilar circuits.

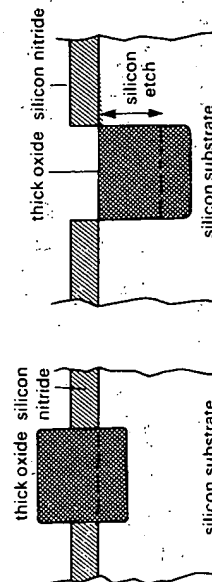
(4) A device, such as a compiler, that changes an information code.

(5) A transducer that converts energy of one type, such as sound waves or electromagnetic radiation, into electrical energy.

Coolidge tube An early form of evacuated X-ray tube.

Cooper pair See superconductivity.

coplanar process *Tradename*: Planox; Isoplanar process; Locos. A technique used during the manufacture of LSI MOS integrated circuits and some forms of LSI bipolar integrated circuits, such as I²L. Regions of relatively thick silicon dioxide are used in order to isolate device areas and to prevent spurious MOST formation. The coplanar process was developed in order to minimize the vertical projection of the oxide layer. A layer of silicon nitride is deposited on the surface of the silicon wafer and is etched to expose the regions of the surface where thick oxide is required. As oxidation takes place, the effective silicon surface moves downwards and is replaced by a thicker layer of silicon dioxide, so that approximately one third of the oxide is below the original exposed surface level (Fig. a). Oxidation may be preceded by etching of the exposed silicon surface so that the final oxide surface is at the same level as the original substrate (Fig. b). The silicon nitride is then removed from the rest of the surface and the integrated circuits are formed using normal planar-process technology.



a Coplanar process with nitride etch b Nitride plus silicon etch

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the case of a planar configuration where the final direction of current flow is parallel to the plane of the metal (see diagram), the contact resistance is defined to be the resistance between the metal and an imaginary plane at the edge of, and perpendicular to the metal, and the *transfer length*, L , is the distance from the edge of the metal at which the current in the semiconductor has fallen to $1/e$ of its original value.

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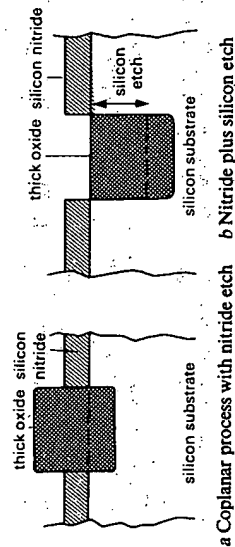
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